SESSION 6 – TAPA I
Strain Enhanced CMOS

Tuesday, June 15, 3:25 p.m.
Chairpersons: Y. Ponomarev, Philips Research Leuven
Y. Omura, Kansai University

6.1 — 3:25 p.m.
35% Drive Current Improvement from Recessed-SiGe Drain Extensions on 37 nm Gate Length PMOS, P.R. Chidambaram, B.A. Smith, L.H. Hall, H. Bu, S. Chakravarthi, Y. Kim*, A.V. Samoilov*, A.T. Kim, P.J. Jones, R.B. Irwin, M.J. Kim**, A.L.P. Rotondaro, C.F. Machala and D.T. Grider, Texas Instruments, Dallas, TX, *Applied Materials, Sunnyvale, CA, **University of Texas at Dallas, Richardson, TX

A novel and manufacturable process that integrates a SiGe epitaxial film at the DE location is demonstrated for the first time. The resulting PMOS transistor at 37 nm gate length is parametrically the best reported (Table 1) device todate. Compressive stress induced in the channel by the SiGe layer at the DE location, is shown to be the major source of the observed 35% performance gain.

6.2 — 3:50 p.m.
Delaying Forever: Uniaxial Strained Silicon Transistors in a 90nm CMOS Technology, K. Mistry, M. Armstrong, C. Auth, S. Cea, T. Coan, T. Ghani, T. Hoffmann, A. Murthy, J. Sandford, R. Shaheed, K. Zawadzki, K. Zhang, S. Thompson and M. Bohr, Intel Corporation, Hillsboro, OR

We describe the device physics of uniaxial strained silicon transistors. Uniaxial strain is more effective, less costly and easier to implement than previous strain techniques. We report the highest PMOS drive current to date:0.72mA/um at 1.2V. Pattern sensitivity and mobility/Rext partitioning are discussed. We describe the implementation of uniaxial strain in a 90nm high volume manufacturing technology. Finally we measure inverter delays as low as4.6pS, and show 50Mb SRAMs operational at 0.65V.

6.3 — 4:15 p.m.
Electron and Hole Mobility Enhancements in Sub-10 nm-thick Strained Silicon Directly on Insulator Fabricated by a Bond and Etch-back Technique, I. Åberg, O.O. Olubuyide, C. Ní Chléirigh, I. Lauer, D.A. Antoniadis, J. Li*, R. Hull* and J.L. Hoyt, MIT, Cambridge, MA, *University of Virginia, Charlottesville, VA

Electron and hole mobilities are studied in strained silicon directly on insulator fabricated by a bond and etch-back technique. For inversion charge densities of 10^13 cm^-2, mobility enhancements of 100% (n-MOSFET, 1.25% strain) and 50% (p-MOSFET, 1.67% strain), are measured. For a biaxial strain level of 1.25%, hole mobility is the same for body thicknesses of 25 and 13 nm, and drops by no more than 5% for a body thickness of 8.5 nm.

6.4 — 4:40 p.m.
MOSFET Current Drive Optimization Using Silicon Nitride Capping Layer for 65-nm Technology Node, S.Pidin, T.Mori, R.Nakamura, T.Saiki, R.Tanabe*, S.Satoh, M.Kase, K.Hashimoto, and T.Sugii, Fujitsu, Ltd., Tokyo, Japan

NMOSFET strain engineering using highly tensile silicon nitride capping layer was studied by way of extensive numerical simulations and device experiments. At 45nm gate length and 1V supply voltage fabricated NMOSFET delivers 1.00mA/micron drive current for off-state current of 40nA/micron and physical gate oxide thickness of 1.25nm(TEM). These data demonstrate the best up to date NMOSFET current drivability. Next, using extensive process simulations to analyze fabricated devices we developed optimization guidelines for NMOSFET strain engineering enabling us further improvement of device current drivability with reducing the gate length.

6.5 — 5:05 p.m.
Stress Memorization Technique (SMT) by Selectively Strained-Nitride Capping for Sub-65nm High-Performance Strained-Si Device Application, C.-H. Chen, T.L. Lee, T.H. Hou, C.L. Chen, C.C. Chen, J.W. Hsu, K.L. Cheng, Y.H. Chiu, H.J. Tao, Y.Jin, C.H. Diaz, S.C. Chen and M.-S. Liang, Taiwan Semiconductor Manufacturing Co., Ltd., Hsin-Chu, Taiwan, ROC

An advanced stress memorization technique is presented. A high-tensile nitride layer is selectively deposited as a temporary stressor to modulate the channel stress. The stress effect was then enhanced and memorized through well-controlled polysilicon amorphorization and re-crystallization procedures. More than 15% NMOS drivability improvement was obtained without PMOS degradation. Device performance can be further enhanced by combing strained contact-etch-stop layer. This simple, reliable and compatible SMT process represents a promising local-strain approach for sub-65nm CMOS application.